

1 : INSULATING SUBSTRATE 2 : SHIFT REGISTER

6: DISPLAY REGION

7: PIXEL TFT

8: PIXEL

**SW: SWITCH CIRCUIT** 

<sup>3 :</sup> DECODER 4 : DA CONVERTER 5 : SCANNING CIRCUIT

FIG.2

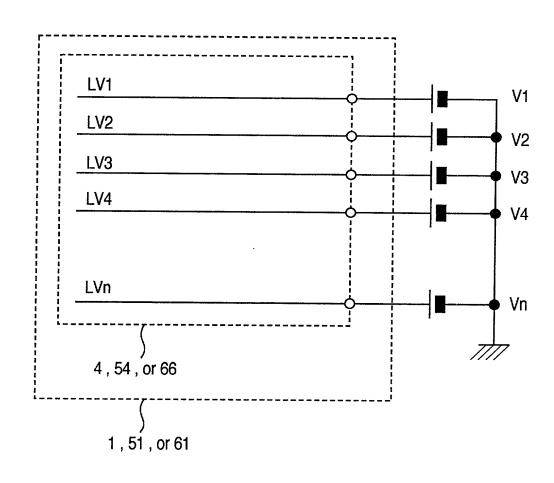


FIG.3

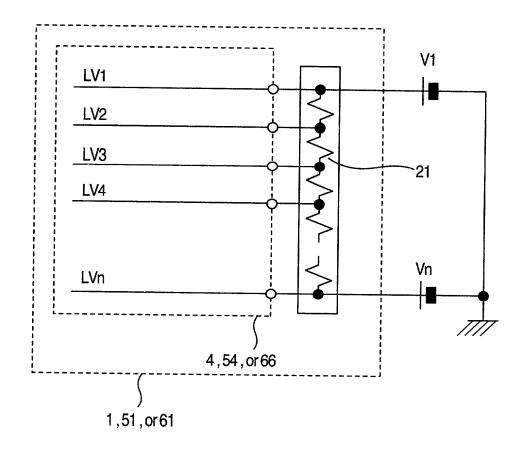


FIG.4

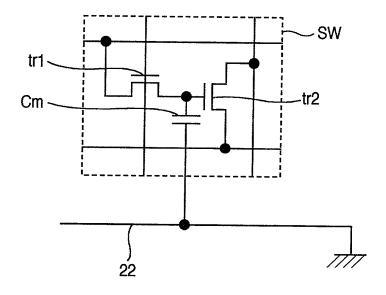


FIG.5

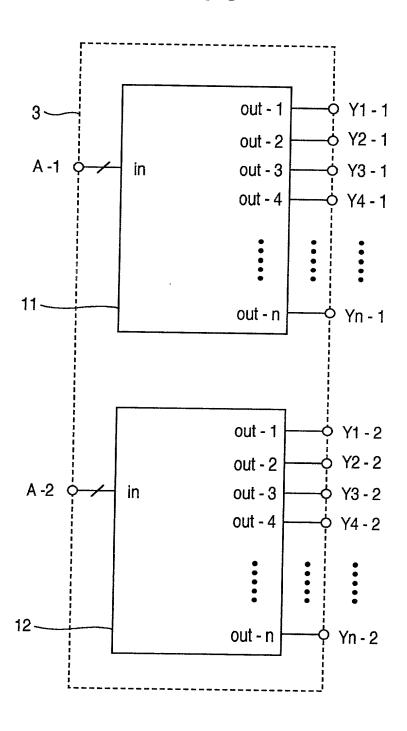


FIG.6

in	out - 1	out - 2	out - 3	out - 4	out - 5	••••	out - n
1	1	0	0	0	0	••••	0
2	0	1	0	0	0	••••	0
3	0	0	1	0	0	••••	0
4	0	0	0	~	0	••••	0
5	0	0	0	0	1	••••	0
•	••••	•••••	•••••	•••••	••••	•••	••••
n	0	0	0	0	0	••••	1

FIG.7

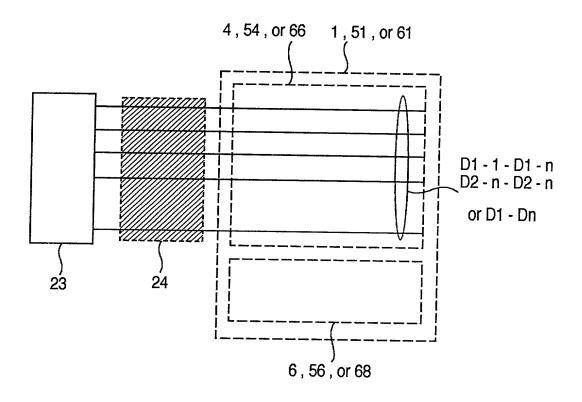
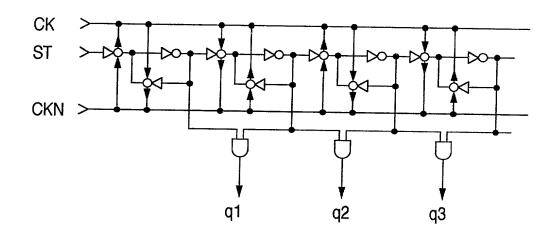


FIG.8



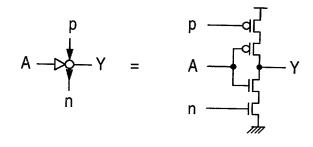
### FIG.9A

**INVERTER** 

$$A \longrightarrow Y = A \longrightarrow Y$$

### FIG.9B

**CLOCKED INVERTER** 



### FIG.9C

AND GATE

FIG.10

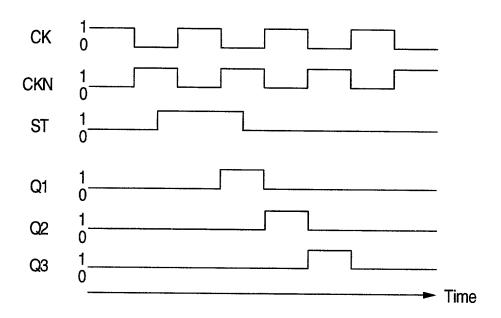


FIG.11

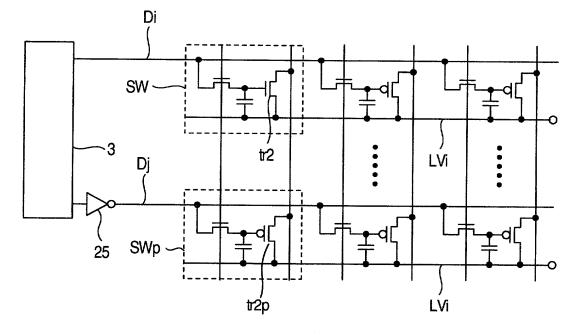


FIG.12

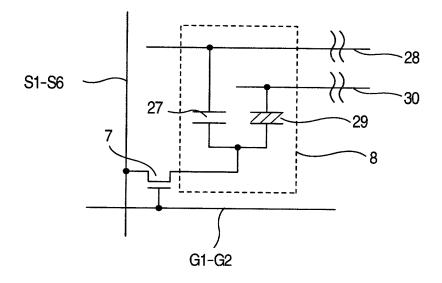


FIG.13

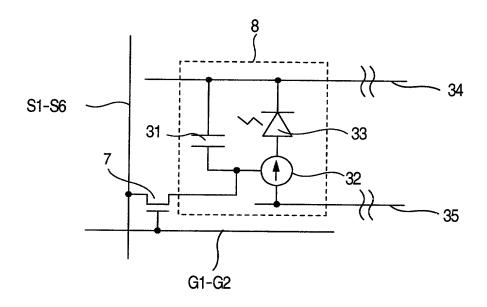


FIG.14

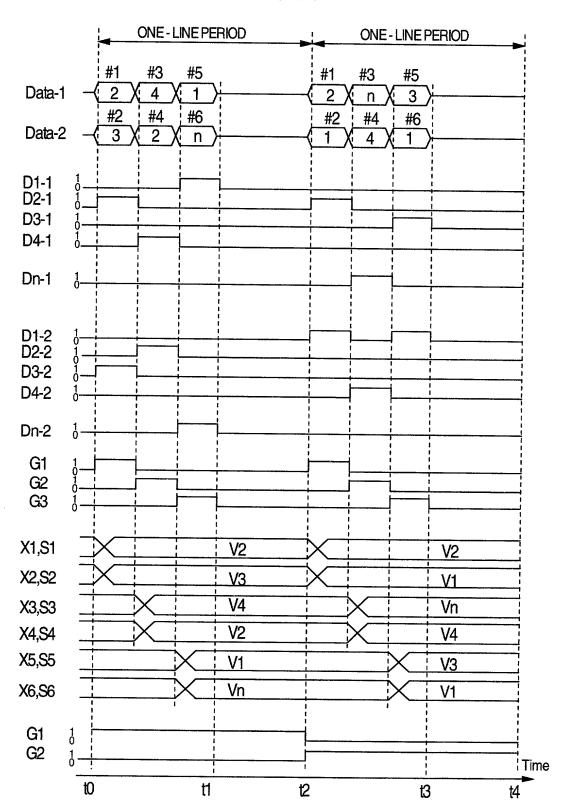


FIG.15

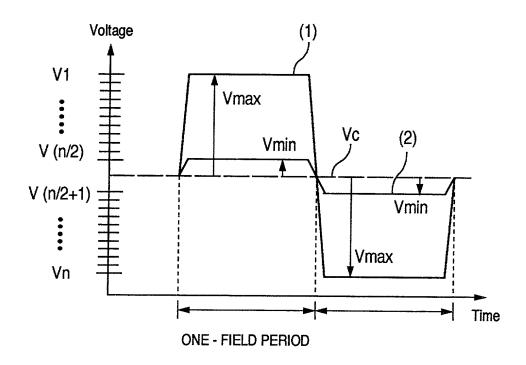


FIG.16

	in	out - 1	out - 2	out - 3	••••	out - n	out - (n/2+1)	••••	out - (n-2)	out - (n-1)	ont - n			
	1	1	0	0	••••	0			•					
	2	0	1	0	••••	0	]							
ppo	3	0	0	1	••••• 0 All 0									
0	•	:	••••	•	٠.,									
	n/2	0	0	0	••••									
	1						0	••••	0	0	1			
	2						0	••••	0	1	0			
Even	3			All	Λ		0	••••	1	0	0			
  回 				<b>/</b> ∖II	U		••••	••••	••••	••••	•			
	n/2	1 •••• 0 0 0								0				

FIG.17

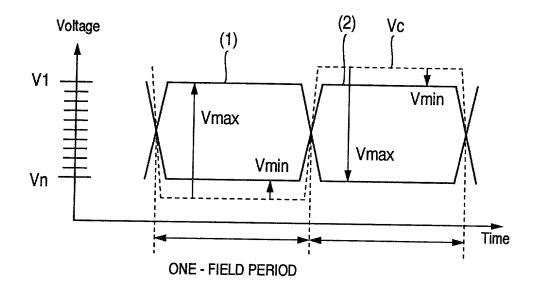
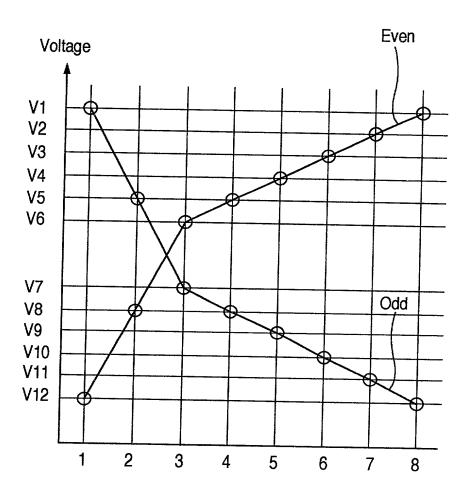


FIG.18



# FIG.19

in	out-1	out-2	out-3	out-4	out-5	ont-6	out-7	out-8	out-9	out-10	out-11	out-12
1	1	0	0	0	0	0	0	0	0	0	0	0
2	0	0	0	0	1	0	0	0	0	0	0	0
	0	0	0	0	0	0	1	0	0	0	0	0
	0	0	0	0	0	0	0	1	0	0	0	0
	0	0	0	0	0	0	0	0	1	0	0	0
	0	0	0	0	0	0	0	0	0	1	0	0
	0	0	0	0	0	0	0	0	0	0	1	0
	0	0	0	0	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	1	0	0	0	0
	0	0	0	0	0	1	0	0	0	0	0	0
4	0	0	0	0	1	0	0	0	0	0	0	0
5	0	0	0	1	0	0	0	0	0	0	0	0
6	0	0	1	0	0	0	0	0	0	0	0	0
7	0	1	0	0	0	0	0	0	0	0	0	0
8	1	0	0	0	0	0	0	0	0	0	0	0
	1 2 3 4 5 6 7 8 1 2 3 4 5 6 7	1 1 2 0 3 0 4 0 5 0 6 0 7 0 8 0 1 0 2 0 3 0 4 0 5 0 6 0 7 0	1 1 0 2 0 0 3 0 0 4 0 0 5 0 0 6 0 0 7 0 0 8 0 0 1 0 0 2 0 0 3 0 0 4 0 0 5 0 0 6 0 0	1 1 0 0   2 0 0 0   3 0 0 0   4 0 0 0   5 0 0 0   6 0 0 0   7 0 0 0   8 0 0 0   1 0 0 0   2 0 0 0   3 0 0 0   4 0 0 0   5 0 0 0   6 0 0 1   7 0 1 0	1 1 0 0 0   2 0 0 0 0   3 0 0 0 0   4 0 0 0 0   5 0 0 0 0   6 0 0 0 0   7 0 0 0 0   8 0 0 0 0   9 0 0 0 0   2 0 0 0 0   3 0 0 0 0   4 0 0 0 0   5 0 0 0 1   6 0 0 1 0   7 0 1 0 0	1 1 0 0 0 0   2 0 0 0 0 0 1   3 0 0 0 0 0 0 0   4 0 0 0 0 0 0 0 0   5 0 0 0 0 0 0 0 0   6 0 0 0 0 0 0 0 0 0   2 0 <	1 1 0 0 0 0 0   2 0 0 0 0 0 0 0   3 0 0 0 0 0 0 0   4 0 0 0 0 0 0 0   5 0 0 0 0 0 0 0   6 0 0 0 0 0 0 0   7 0 0 0 0 0 0 0   8 0 0 0 0 0 0 0   8 0 0 0 0 0 0 0   1 0 0 0 0 0 0 0   2 0 0 0 0 0 0 0   3 0 0 0 0 0 0 0   4 0 0 0 0 0 0 0   5	1 1 0	1 1 0	1 1 0	1 1 0	1 1 0

## FIG.20

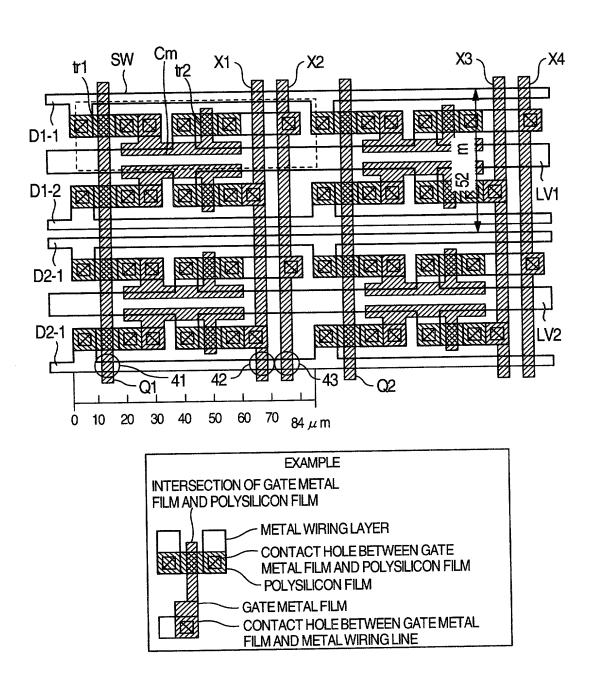


FIG.21

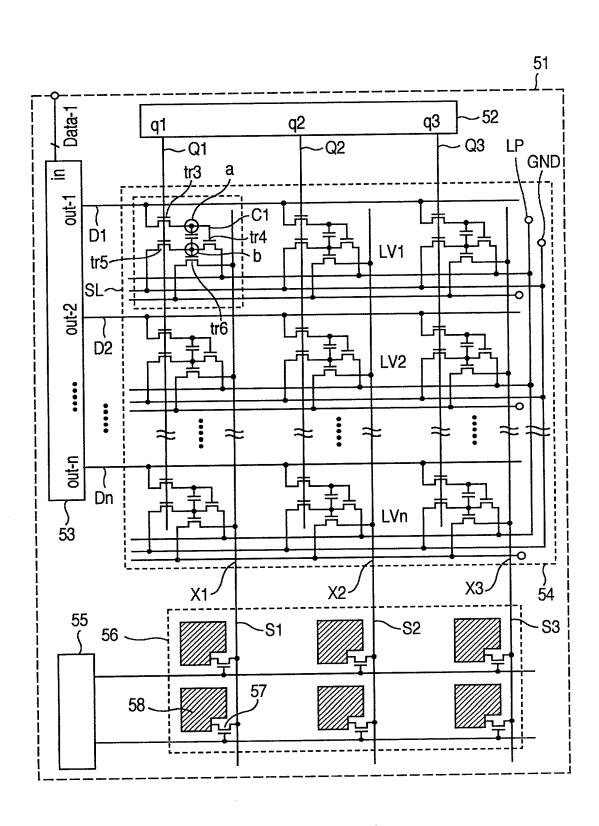


FIG.22

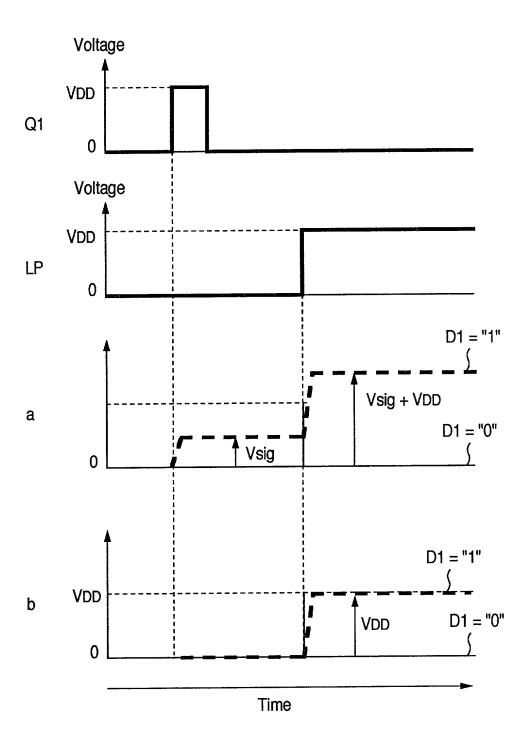


FIG.23

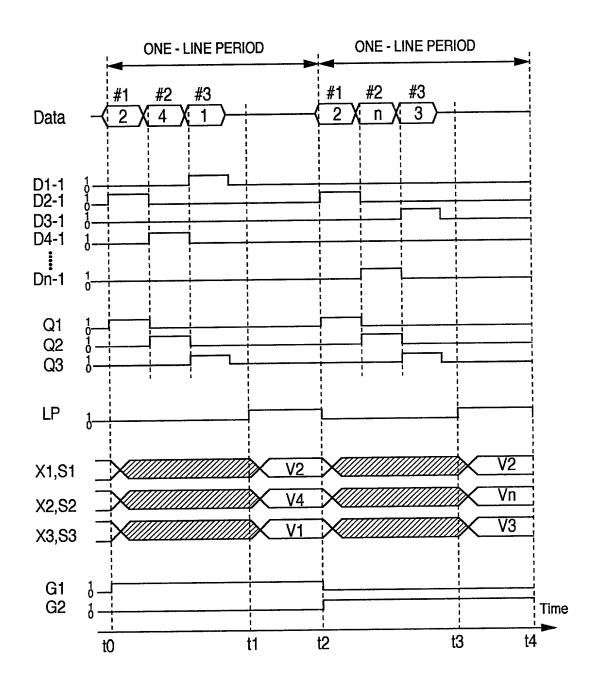


FIG.24

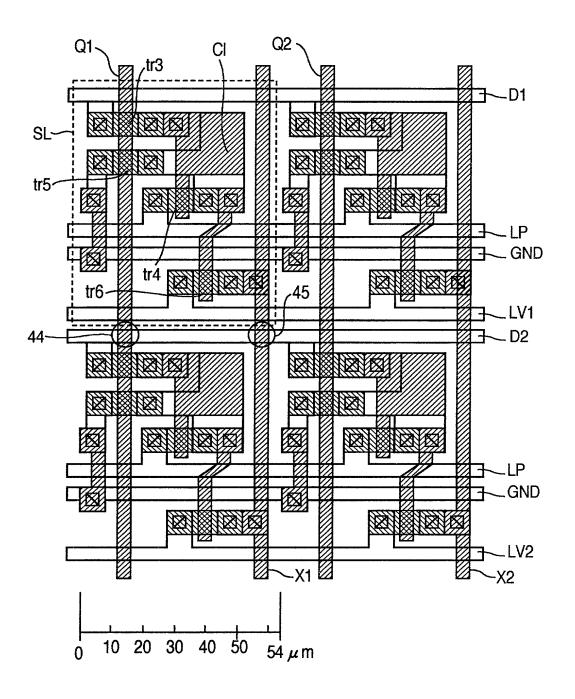


FIG.25

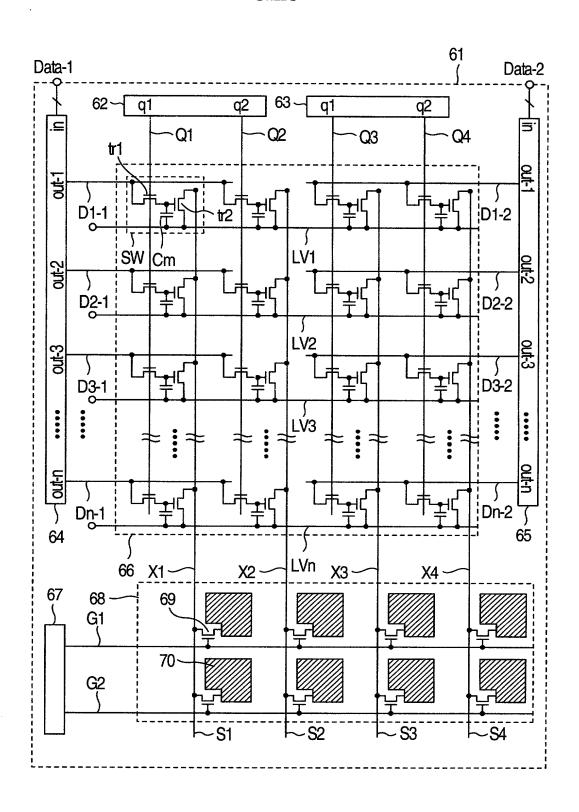


FIG.26

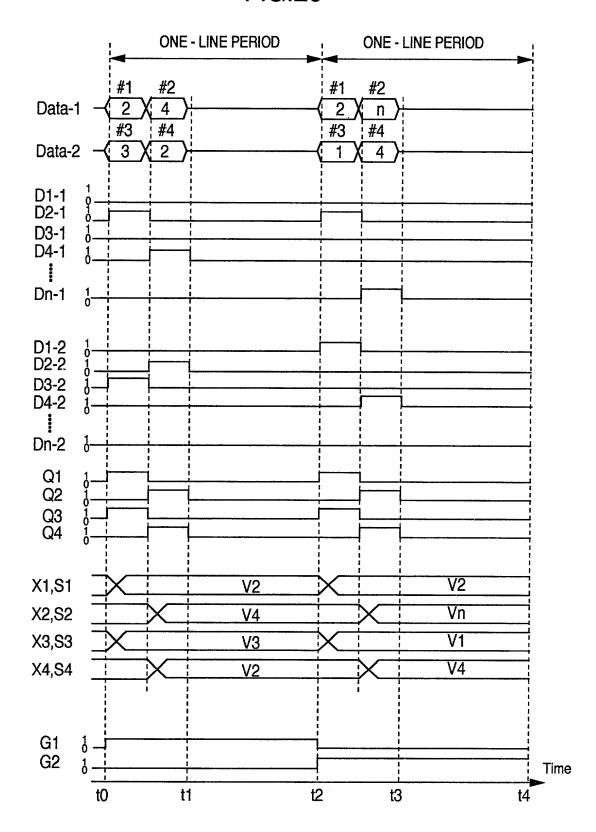


FIG.27

